REMARKS

Claims 20-27 are pending. Claims 20-27 have been amended by way of the present amendment. Reconsideration is respectfully requested.

In the outstanding Office Action, claims 20 and 23 were objected to because of informalities; claims 21, 23 and 26 were rejected under 35 U.S.C. §112, 2nd paragraph, as indefinite; claims 20-27 were rejected under 35 U.S.C. §102 (b) as being anticipated U.S. Patent No. 5,241,210 (Nakagawa et al.); and claims 20-27 were rejected under 35 U.S.C. §102 (e) as being anticipated U.S. Patent No. 5,241,210 (Yamaguchi et al.).

Claim Objections

In response to the objection to claims 20 and 23 due to informalities, the typographical errors in each claim have been corrected in order to change the word "is" to "in." Applicant respectfully submits the amendments raise no question of new matter.

Claim Rejections - 35 U.S.C. §112

In response to the rejection of claims 21, 23 and 26 under 35 U.S.C. §112, 2nd paragraph, claims 21 and 23 have been amended to clarify the invention. In particular, claim 21 has been amended to provide antecedent basis for the term "gate" and claim 23 has been amended to recite the term "region" instead of "layer." Further, claim 26 has been amended to recite:

> [a] method for making a semiconductor chip comprising:
> forming multiple diffusion regions that are surrounded by multiple trench structures on a substrate;
> ~~forming multiple diffusion regions in said trench structures in said substrate~~; and
> forming multiple contacts on each of said trench structures and said substrate for controlling current through said diffusion regions.

Applicants respectfully submit that the amendments are supported by the specification and Figures of the application. Specifically, the outstanding Office Action, at page 4, lines 3-4,

has indicated that "trenches surround the diffusion region." Therefore, it is respectfully submitted that the amendments raise no question of new matter and that the amended claims are definite.

Claim Rejections - 35 U.S.C. §102

Claims 20-27 were rejected under 35 U.S.C. §102 (b) as being anticipated U.S. Patent No. 5,241,210 (Nakagawa et al.). Applicants respectfully traverse.

Nakagawa et al. discloses a high breakdown voltage semiconductor device.[1] In particular, Nakagawa et al. discloses a first semiconductor region **54a** isolated by oxide films **52a** and **53a** formed on a substrate **51**.[2] In addition, Nakagawa et al. discloses a fifth semiconductor region **59a** that is formed on a bottom portion of the first semiconductor region **54a** and contacting oxide film **52a**.[3] Further, Nakagawa et al. discloses a first and second electrodes **62a, 63a** as source and drain electrodes, respectively, on layers **58a** and **57a** in a peripheral portion of the first semiconductor region **54a**.[4] Moreover, Nakagawa et al. discloses that the gate electrode **61** is formed on a surface portion of a fourth semiconductor layer **57**.

However, Nakagawa et al. nowhere discloses, as recited in claim 20, that:

> forming electrical connections on said trench structure and said substrate which *receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region* (emphasis added).

In addition, claim 26, recites:

> forming multiple contacts on each of said trench structures and said substrate *for controlling current through said diffusion regions* (emphasis added).

That is, as discussed above, Nakagawa discloses a gate electrode **61** or control electrode formed on the fourth semiconductor layer **57**. Moreover, the outstanding Office Action

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[1] Nakagawa et al. at ABSTRACT.
[2] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.
[3] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.
[4] *Id.* at FIG. 6; FIG. 17; column 7, lines 25-46; column 9, lines 36-49.

indicates that the "trench structure" of the claimed invention is analogous to the oxide film **53/53a** of FIG. 6/FIG. 17.[5] In contrast to Nakagawa, claim 20 recites: "forming electrical connections on said trench structure," *such as a gate or control electrode*, and "which receive a control voltage." Applicants respectfully submit that the "control electrode" disclosed by Nakagawa is *not* formed on the "trench structure," as recited in claims 20 and 26.

Therefore, it is respectfully submitted that Nakagawa does not disclose, anticipate or inherently teach the claimed invention and that claims 20 and 26, and claims dependent thereon, patentably distinguish thereover.

Claims 20-27 were rejected under 35 U.S.C. §102 (b) as being anticipated U.S. Patent No. 6,118,152 (Yamaguchi et al.). Applicants respectfully traverse.

Yamaguchi et al. discloses a silicon layer provided in a silicon substrate through a buried oxide film that includes a silicon island partitioned by a trench.[6] In particular, Yamaguchi et al. discloses oxide films **13a, 13b** formed between drain region **9** and well regions **10a, 10b**, respectively.[7] Further, Yamaguchi et al. discloses forming gate electrodes **15a, 15b** over the well regions **10a, 10b.**[8] Moreover, Yamaguchi et al. discloses a trench **5** surrounding a silicon island **8.**[9]

However, Yamaguchi et al. nowhere discloses, as recited in claim 20, that:

> *forming electrical connections on said trench structure* and said substrate which receive a control voltage whereby an electric field is produced to control a current flowing in said diffusion region (emphasis added).

In addition, claim 26, recites:

> *forming multiple contacts on each of said trench structures* and said substrate for controlling current through said diffusion regions (emphasis added).

That is, as discussed above, Yamaguchi et al discloses a trench **5** surrounding a silicon island **8.** In contrast to Yamaguchi et al., claim 20 recites: "forming electrical connections

[5] Office Action at page 2, paragraph 2, lines 4-7.
[6] Yamaguchi et al. at ABSTRACT.
[7] *Id.* at column 3, line 43 to column 4, line 53.
[8] *Id.* at column 3, line 43 to column 4, line 53.
[9] *Id.* at column 3, line 43 to column 4, line 53.

on said trench structure," *such as a gate or control electrode*, and "which receive a control voltage." Applicants respectfully submit that the "control electrode" (i.e., gate electrodes **15a, 15b**) disclosed by Yamaguchi et al. are *not* formed on the "trench structure," as recited in claims 20 and 27 but are instead formed on oxide films **13a, 13b**, which are *not* analagous to the recited "trench structure" of the claims

Therefore, it is respectfully submitted that Yamaguchi et al. does not disclose, anticipate or inherently teach the claimed invention and that claims 20 and 27, and claims dependent thereon, patentably distinguish thereover.

Conclusion

In view of the above amendments and remarks, reconsideration and allowance of the pending claims are respectfully requested.

Applicants believe that the present application is in condition for allowance, and an early indication of the same is respectfully requested.

If the Examiner has any questions or requires clarification, the Examiner may contact the undersigned so that this Application may continue to be expeditiously advanced. In the event the Examiner believes an interview might serve to advance the prosecution of this application in any way, the undersigned is available at the telephone number noted below.

The Director is hereby authorized to charge any fees, or credit any overpayment, associated with this communication, including any extension fees, to Deposit Account No. 22-0185.

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Respectfully submitted,

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